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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,188	01/15/2002	Brian C. Barnes	2000.056900/TT4089	5070
23720	7590	05/13/2005		
WILLIAMS, MORGAN & AMERSON, P.C. 10333 RICHMOND, SUITE 1100 HOUSTON, TX 77042			EXAMINER SON, LINH L D	
			ART UNIT 2135	PAPER NUMBER
DATE MAILED: 05/13/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/047,188

Applicant(s)

BARNES ET AL.

Examiner

Linh LD Son

Art Unit

2135

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 February 0115.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/02, 05/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This written action is responding to the application filed on 01/15/2002.
2. Claims 1-20 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by England et al, US Patent No. 6775779B1, hereinafter England.
5. As per claims 1 and 12, England discloses “A method, comprising: executing a software object; establishing a security level for said software object” in (Col 9 lines 42-50 and Col 10 lines 6-20); “performing a multi-table input/output (I/O) space access using at least one of said security levels; and executing said function of said object” in (Col 5 lines 55-67).
6. As per claims 2, 9, and 18, England discloses “The method described in claims 1, 8, and 17, wherein executing a software object further comprises using a processor to process software code of said software object” in (Col 8 lines 10-24).

7. As per claims 3, 10, and 19, England discloses “The method described in claims 1, 8, and 17, wherein establishing a security level for said software object further comprises assigning a security level relating to a input/output (I/O) space access of at least a portion of a input/output (I/O) space” in (Col 5 lines 55-67).

8. As per claim 4, England discloses “The method described in claim 1, wherein performing a multi-table input/output (I/O) space access using at least one of said security level further comprises: establishing a secondary table; receiving a input/output (I/O) space access request based upon executing of said software object; performing a multi-level table access based upon said input/output (I/O) space access request using said secondary table and at least one virtual input/output (I/O) space table; and accessing a portion of a input/output (I/O) device based upon said multi-level table access” in (Col 6 lines 33-45).

9. As per claim 5, England discloses “The method described in claim 4, wherein establishing a secondary table further comprises: dividing a physical input/output (I/O) space into a plurality of segments; determining at least one of said segment to omit from said secondary table and at least one un-omitted segment; assigning a default security level to said omitted segment; assigning a security level to said un-omitted segment; and correlate at least one assigned segment with a virtual input/output (I/O) space location” in (Col 6 lines 33-45, and lines 46-65).

10. As per claims 6 and 20, England discloses “The method described in claims 4 and 17, wherein performing a multi-level table access based upon said input/output (I/O) space access request further comprises: determining at least one security level that corresponds to a segment in said secondary table” in (Col 6 lines 33-40); “verifying a match between an execution security level to a security level associated with a segment being accessed in response to an execution of said object” in (Col 6 lines 40-45); “determining a virtual input/output (I/O) space address based upon said secondary table in response to a match between said execution security level and said security level associated with said segment being accessed; and locating a input/output (I/O) device corresponding to said virtual input/output (I/O) space address” in (Col 6 lines 46-65, and Col 10 lines 40-50)

11. As per claims 7, and 11, England discloses “The method described in claims 6, and 8, wherein determining at least one security level that corresponds to a segment in said secondary table comprises: determining a physical I/O device address from said virtual input/output (I/O) space table” in (Col 10 lines 40-50, and Col 6 lines 55-65); “determining a segment being executed based upon said physical address; and defining a current security level based upon said determining of said segment being executed” in (Col 6 lines 46-65).

12. As per claims 8 and 17, England discloses “A method, comprising: executing a software object; establishing a security level for said software object” in (Col 9 lines 42-50 and Col 10 lines 6-20); “establishing a secondary input/output (I/O) table; receiving a input/output (I/O) space access request based upon said executing of said software object” in (Col 6 lines 33-45);

“determining at least one security level that corresponds to a segment in said secondary table” in (Col 6 lines 33-45, and lines 46-65); “verifying a match between an execution security level to a security level associated with a segment being accessed in response to an execution of said software object” in (Col 12 lines 25-39); “determining a virtual input/output (I/O) space address based upon said secondary input/output (I/O) table in response to a match between said execution security level and said security level associated with said segment being accessed” in (Col 6 lines 46-65, and Col 10 lines 40-45); “locating a physical input/output (I/O) device location corresponding to said virtual input/output (I/O) space address; and accessing a portion of a input/output (I/O) device based upon locating said physical input/output (I/O) space location” in (Col 6 lines 46-65).

13. As per claims 13-14, England discloses “An apparatus, comprising: a processor coupled to a bus; means for coupling at least one software object to said processor; a input/output (I/O) device unit; and a input/output (I/O) access interface coupled to said bus and said input/output (I/O) space unit” in (Col 4 lines 15-35), “said input/output (I/O) space access interface to provide said processor a multi-level table input/output (I/O) space access of at least a portion of said input/output (I/O) space unit based upon at least one security level, in response to said processor executing said software object” in (Col 5 lines 55-67).

14. As per claim 15, England discloses “The apparatus of claim 13, wherein said input/output (I/O) space access interface comprises a virtual input/output (I/O) space access table coupled with a secondary input/output (I/O) table, said input/output (I/O) space access interface to

provide a virtual input/output (I/O) space addressing scheme to access at least one portion of said input/output (I/O) device based upon a security level” in (Col 6 lines 45-65, and Col 10 lines 40-50).

15. As per claim 16, England discloses “The apparatus of claim 13, wherein said input/output (I/O) device comprises at least one of a magnetic tape memory, a flash memory, a random access memory, and a memory residing on a semiconductor chip” in (Col 4 lines 25-35).

Double Patenting

16. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

17. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

18. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

19. Claims 1-20 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09999881, hereinafter '881. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-20 in this application recites similar feature as the claims 1-20 in the copending Application '881, except the copending Application '881 recites "the multi-table input/output (I/O) space" feature in this application as the "the multi-table memory". Nevertheless, it obvious at the time of the invention was made for one having ordinary skill in the art to interpret the "the multi-table Input/Output space" as the "the multi-table memory". The claimed input/output (I/O) space in this application is referring to the computer readable storage medium, which allows the processor to write or read information from, or input or output information from. The depend claim 16 in both application recites exact similar limitation of the input/output (I/O) space device or memory device.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

20. "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated** by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at

issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). “ ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Conclusion

21. Any inquiry concerning this communication from the examiner should be directed to Linh Son whose telephone number is (571)-272-3856.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Kim Y. Vu can be reached at (571)-272-3859. The fax numbers for this group are (703)-872-9306 (official fax). Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (571)-272-2100.

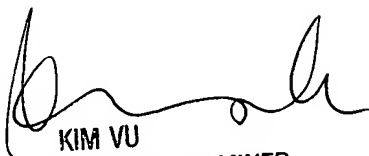
23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval IPAIR.I system. Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PAIR

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system, see <http://pzd-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh LD Son

Patent Examiner



KIM VU
SUPERVISORY PATENT EXAMINER
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